

INTERCONNECT STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation-in-part of prior applications Ser. No. 09/389,823,
5 filed Sep. 3, 1999 and Ser. No. 09/545,651, filed Apr. 10, 2000.

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to a semiconductor device. More particularly, the
10 present invention relates to a structure of a multilevel interconnect.

Description of Related Art

The current integrated circuit device includes not only a field effect transistor (FET) and a bipolar device formed on the semiconductor substrate, but also a multilevel
15 interconnect structure formed on the device. Different devices on the substrate can be connected by means of the multilevel interconnect structure. Among many integrated circuits, the multilevel interconnect structure extends in parallel with one or more arrays of conducting wires, while providing the function of the conducting wires in the devices formed by high integration stacking. When the size of the device is shrunk, an
20 intermetal capacitance between the conducting wires obviously increases. As the data is transmitted with the conducting wires, unnecessary capacitive and inductive couplings are produced between the adjacent conducting wires in a narrow space. Such capacitive and inductive couplings reduce the speed for data transmission,

especially during high-speed data transmission, while the increased energy consumption in this case also limits the efficiency of the device.

Referring to Fig. 1, an air gap 106 is formed in a dielectric layer between the conducting wires 102 in order to reduce the capacitive and inductive couplings between the multilevel interconnects. As the air has a smaller dielectric constant (about 1), the inter-metal dielectric (IMD) made with the air gap between the multilevel interconnects can reduce the dielectric constant and the capacitance between the parallel conducting wires, while improving the data transmission speed and the device efficiency.

Since a misalignment or an increase in critical dimension (CD) of an unlanded via opening (not shown) may occur during the formation of via opening 112, it is not easy to control an etching stopping point when the dielectric layers 110, 108, and 104 are made of similar materials. As a result, the via opening 112 can easily penetrate through the dielectric layers 110, 108, and 104, so that the air gap 106 is breached, resulting in an opening 106a extending from the via opening 112 and the air gap 106. The air gap 106 is not easily filled with a barrier layer 114, when the barrier layer 114 is formed by chemical vapor deposition (CVD) to cover the dielectric layer 110 and the profile of the via opening 112. Therefore, the reactant gas WF_6 diffuses into the air gap 106 and reacts with the oxide in the dielectric layer, producing a poisoned via in the subsequent step for forming the tungsten plug (not shown).

SUMMARY OF THE INVENTION

The invention provides a structure of an interconnect that is briefly described as follows. A conductive structure is formed on a substrate. The conductive structure at least includes a first conductive structure and a second conductive structure, which have

a gap region in-between. The substrate is exposed at the gap region. A first structured dielectric layer is formed over the substrate to cover the first and the second conductive structures. The first structured dielectric layer also has a void at the gap region between the first and the second conductive structures. The void significantly
5 extends to the whole gap region. The first structured dielectric layer also has an indent region above the void. An anti-etch layer fills the indent region of the first structured dielectric layer. As a result, the first structured dielectric layer has a substantially planar surface. A second structured dielectric layer is formed on the first structured dielectric layer and the anti-etch layer. The first structured dielectric layer and the
10 second structured dielectric layer also have an opening to expose the conductive structure. When the opening is shifted to the gap region between the first conductive structure and the second conductive structure due to misalignment, the portion of the opening above the gap region stops on the anti-etch layer without opening the void.

In the foregoing, the gap region between the first conductive structure and the
15 second conductive structure do optionally extend into the substrate, so that a dimension of the void is increased.

The first structured dielectric layer further includes a cap dielectric layer on the conductive structure, wherein the opening also penetrates the cap dielectric layer.

The first structured dielectric layer further includes a liner layer over the
20 substrate, conformal to a topographic surface of the conductive structure and the substrate.

The invention also provides another interconnect structure. A conductive structure is formed on a substrate. The conductive structure at least includes a first conductive structure and a second conductive structures. A cap dielectric layer is

formed on the conductive structure. The first conductive structure and the second conductive structure are separated by a gap region in-between. A first dielectric layer is formed over the substrate to cover the first and the second conductive structures with the doped dielectric layer. The first dielectric layer has a void at the gap region
5 between the first and the second conductive structures. The void significantly extends to the whole gap region. The first dielectric layer also has an indent region above the void. A second dielectric layer is formed on the first structured dielectric layer, in which the indent region is filled. The first dielectric layer and the second dielectric layer also have an opening to expose the conductive structure, wherein the cap dielectric
10 layer is penetrated. When the opening is shifted to the gap region between the first conductive structure and the second conductive structure due to misalignment, the portion of the opening above the gap region stops in the first dielectric layer without opening the void.

In the foregoing, the gap region optionally extends into the substrate, whereby
15 the dimension of the void is increased.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

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BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

Fig. 1 is a schematic diagram illustrating the via opening which penetrates the first dielectric layer and connects to the air gap when misalignment occurs in the prior art;

5 Figs. 2A to 2E are cross-sectional views, schematically illustrating a method for fabricating an interconnect according to a first preferred embodiment of the invention;

Fig. 3 is schematic diagram illustrating the via opening when misalignment occurs

Fig. 3A is schematic diagram illustrating another interconnect structure according to the first preferred embodiment of the invention;

10 Figs. 4A-4B are cross-sectional views, schematically illustrating a method to form an interconnect, according to a second preferred embodiment of the invention;

Figs. 5A-5C are cross-sectional views, schematically illustrating a method to form an interconnect, according to a third preferred embodiment of the invention;

15 Figs. 6A-6D are cross-sectional views, schematically illustrating a method to form an interconnect, according to a fourth preferred embodiment of the invention;

Figs. 7A-7B are cross-sectional views, schematically illustrating a method to form an interconnect, according to a fifth preferred embodiment of the invention; and

20 Figs. 8A-8B are cross-sectional views, schematically illustrating a method to form an interconnect with increased void size, according to the fifth preferred embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention particularly forms a void between conductive structures of an interconnect by depositing a dielectric layer with loose step coverage. The void is

intended to be sufficiently large to effectively reduce at least the parasitic capacitance on the inter-metal dielectric layer. Several embodiments are to be described.

First embodiment

5 Figs. 2A to 2E are cross-sectional views, schematically illustrating a method for fabricating the multilevel interconnect according to the preferred embodiment of the invention.

Referring to Fig. 2A, a substrate formed with semiconductor devices (not shown) is provided. A conductive structure is formed on the substrate 200. The
10 conductive structure includes at least two sub-conductive structures, such as conducting wires 202a, 202b, 202c, formed on the substrate 200. The conducting wires 202a, 202b, 202c usually form one level of a multilevel interconnect of the device. The conductive structure includes, for example, doped polysilicon or metal materials such as aluminum, copper, tungsten, metal or metal alloy thereof. For a clear description, the
15 conducting wires 202a, 202b, 202c can also be briefly numbered as the conductive structure 202. The conductive wires 202a, 202b, 202c are separated by a gap region. A dielectric layer 204 is formed to cover the substrate 200 and the conductive structure 202, wherein a void 206 is formed in the dielectric layer 204 at the gap region between the conducting wires 202a, 202b, 202c. The void 206, for example, is formed due to
20 requiring a loose step coverage or even a poor step coverage. As a result, the void 206 significantly extends to the whole gap region. Preferably, the dielectric layer 204 includes silicon oxide or doped oxide. The dielectric layer 204 can be formed by plasma enhanced chemical vapor deposition (PECVD), and has a thickness approximately between 2000-4000Å. A thickness of 3000Å on the conducting wires

202 is preferred. When the gap region between the conducting wires 202a, 202b, 202c is filled with the dielectric layer 204 made from the material resulting poor step coverage, an overhang is formed on the top corners of the conductive wires 202a, 202b, 202c. This makes it difficult to fill the whole space of the gap region. The overhangs
5 on the corners close the gap region and forms the void 206 in the dielectric layer 204 at the gap region. Due to the gap region, the dielectric layer 204 also has an indent region above the void 206.

Referring to Fig. 2B, an anti-etch layer 207 is formed on the dielectric layer 204, wherein the anti-etch layer 207 has a smaller etching rate than the dielectric layer 204.
10 The anti-etch layer 207 is preferably made of, for example, silicon nitride, aluminum oxide, aluminum nitride, titanium oxide, silicon carbide, and aluminum silicate formed by chemical vapor deposition (CVD) such as PECVD or photo-induced chemical vapor deposition (PICVD).

Referring to Fig. 2C, a part of the anti-etch layer 207 is removed until a part of
15 the dielectric layer 204 is exposed, so that a remaining anti-etch layer 207a fills the indent region. The anti-etch layer 207a in general is a mask layer to mask the void 206 as can be seen later. To remove the part of the anti-etch layer 207, a planarization process, such as a chemical mechanical polishing (CMP) process or an etching back process, is employed. The anti-etching layer 207a has its function to stop an etching
20 process in the subsequent process as is to be described later.

In general, the anti-etch layer is not only formed by using the foregoing mechanism even though it is more simple. The anti-etch layer over the void 206 can be formed by directly patterning the anti-etch layer by an additional photolithography

step. In this manner, the geometric structure of the anti-etch layer 207a is different. For example, it may be a damascened layer in the dielectric layer 204 over the void 206.

Referring to Fig. 2D, a dielectric layer 211 is formed on the dielectric layer 204 and the anti-etch layer 207a. The dielectric layer 211, for example, can include multiple layers 208, 210 sequentially formed on the substrate 200. The dielectric layer 211 have a larger etching rate than the anti-etch layer 207a. The dielectric layer 208 may include the silicon oxide layer formed by high-density plasma chemical vapor deposition (HDPCVD), while the dielectric layer 210 may include the silicon oxide layer formed by plasma enhanced chemical vapor deposition (PECVD).

Referring to Fig. 2E, the dielectric layers 211, 204 are patterned to form an opening 212, such as a via, which penetrates dielectric layers 211, 204 and exposes, for example, the conducting wire 202b. A barrier layer 214 is then formed to cover a peripheral surface of the opening 212, where the barrier layer 214 contact the exposed portion of the conductive wire 202b. The barrier layer 214 may include a titanium/titanium nitride layer. A via plug is formed to fill the via opening 212, wherein the via plug may be a tungsten plug.

Referring to Fig. 3, if a misalignment occurs during the formation of the opening, a misaligned opening 312 is formed. The opening 312 is shifted to the gap region. In Fig. 3, the elements with the same reference numbers represent the same elements in Fig. 2E. Since the anti-etch layer 207a has a smaller etching rate relative to the dielectric layer 204. In other words, the anti-etch layer 207a is a mask layer serving as an etching stop. As a result, the portion of the opening 312 above the gap region stops on the anti-etching layer 207a or just an upper portion of the anti-etching

layer 207a being etched without opening the void 206. The void 206 reduces the parasitic capacitance in the inter-metal dielectric layer of the interconnecting structure.

Fig. 3A is schematic diagram illustrating another interconnect structure according to the first preferred embodiment of the invention. The anti-etch layer 207b over the void 206 is formed by directly patterning the anti-etch layer by an additional photolithography step. In this manner, the geometric structure of the anti-etch layer 207b is different and met requirements of designs. Furthermore, it can also be a damascened layer in the dielectric layer 204 over the void 206.

10 Second embodiment

Figs. 4A-4B are cross-sectional views, schematically illustrating a method to form an interconnect, according to a second preferred embodiment of the invention. The second embodiment is similar to the first embodiment. The difference is that the gap region now extends into the dielectric layer. As a result, the dimension of the void is increased. In Fig. 4A, the conductive structure 402 is formed on the substrate 400. The conductive structure 402 can include at least two sub-conductive structures, such as metal wires. When the conductive structure 402 is patterned, the substrate 400 is also etched by a distance of "d". The substrate 400 usually includes a device formed thereon. Typically, an insulating layer is formed on the top for supporting the conductive structure 402. Then, a dielectric layer 404 is formed over the substrate 400. With the same mechanism as described in the first embodiment, a void 406 is formed in the dielectric layer 404 at the gap region in the conductive structure 402. The dielectric layer 404 also has an indent region above the void 406. A mask layer, such as an anti-etch layer 408, fills the indent region. Since the gap region extends in to the

substrate 400, the dimension of the void 406 is increased. A dielectric layer 410 is formed on the dielectric layer 404 and the anti-etch layer 408.

In Fig. 4B, the dielectric layers 404, 410 are patterned to form an opening 412, which exposes the conductive structure 402. If misalignment occurs, the opening 412 shifts into the gap region. Since the anti-etch layer 408 has less etching rate, serving as an etching stop or a mask, the portion of the opening 412 above the gap region stops on the anti-etch layer 408 without opening the void 406. In this embodiment, since the gap region extends into the dielectric layer, the dimension of the void 406 is increased. The parasitic capacitance of the interconnect is further reduced.

Third embodiment

Figs. 5A-5C are cross-sectional views, schematically illustrating a method to form an interconnect, according to a third preferred embodiment of the invention. In Fig. 5A, a conductive layer is formed on a substrate 500 and is patterned into a conductive structure 502. After patterning, the conductive structure 502 has a gap region 520, which expose the substrate 500. A liner layer 504 is formed over the substrate, conformal to a topographic surface over the substrate 500. The liner layer 504 includes, for example, oxide, nitride, silicon oxynitride, tantalum, tantalum nitride, titanium or titanium nitride.

Similar to the previous embodiment, a dielectric layer 506 is formed over the substrate on the liner layer 504 as shown in Fig. 5B. With the same mechanism, the dielectric layer 506 has a void 508 in the gap region 520. Preferably, the dielectric layer 506 includes silicon oxide or doped oxide. The dielectric layer 506 can be

formed by plasma enhanced chemical vapor deposition (PECVD), and has a thickness approximately between 2000-4000Å.

The dielectric layer 506 also has an indent region above the void 508. The indent region is filled with an anti-etching layer 510. A dielectric layer 512 is formed
5 on the dielectric layer 506 and the anti-etch layer 510.

In Fig. 5C, the dielectric layers 510, 512 are patterned to form an opening 514 that exposes the conductive structure 502, where the liner layer 504 is also penetrated by the opening 514. If the opening 514 is misaligned, a portion of the opening 514 has overlapped over the gap region 520. Due to the anti-etch layer 510 in the indent region,
10 the opening 514 also exposes the anti-etch layer 510 and stops there. The anti-etch layer 510 could be also etched a little without significant portion. The void 508 is not open by the opening 514.

Moreover, the gap region 520 in Fig. 5A can also extend into the substrate like the structure in FIG. 4A without a problem. Also and, the liner layer 504 can be also
15 formed by thermal oxidation on the exposed surface of the conductive structure if the conductive structure 502 includes polysilicon.

Fourth embodiment

Figs. 6A-6D are cross-sectional views, schematically illustrating a method to
20 form an interconnect, according to a fourth preferred embodiment of the invention. In Fig. 6A, a conductive layer 602 and a dielectric layer 604 are sequentially formed on a substrate 600, which may have a device already formed thereon. The dielectric layer 604 includes a material that has a different etching rate from that of an inter-metal dielectric layer. Preferably, the dielectric layer 604 has greater etching rate than the

inter-metal dielectric layer. The dielectric layer 604 has at least advantages of increasing the void size and allows a self-aligned features as to be described later. In order to have the greater etching rate, the dielectric layer 604 preferably can include a doped dielectric material, which has greater etching rate than an undoped dielectric material. The doped dielectric layer 604 includes, for example, phosphosilicate glass (PSG) or Borophosphosilicate glass (BPSG).

In Fig. 6B, the dielectric layer 604 and the conductive layer 602 are patterned to form a conductive structure 602a. The dielectric layer 604a is formed on the conductive structure 602. The conductive structure 602a has a gap region 605 to expose the substrate 600. Similarly, the gap region 606 may optionally extend into the substrate by a distance of "d" during patterning. Also and, a liner layer like the one in Fig. 5A can also be optionally formed on the conductive structure 602 or also on the dielectric layer 604a and the substrate 600 within the gap region 605. The dielectric layer 604 can also be called as a cap layer 604.

In Fig. 6C, a dielectric layer 606 is formed over the substrate 600 to cover the conductive structure 602 with the cap layer 604. With the same mechanism, a void 608 exists in the gap region 606, and an anti-etch layer 610 fills the indent region of the dielectric layer 606. The cap layer 604 provides an additional height to have larger void 608. This is one of features in this embodiment. A dielectric layer 612 is formed on the dielectric layer 606 and the anti-etch layer 610.

In Fig. 6D, the dielectric layers 612 and 606 are patterned to form an opening 614. The cap layer 604 is continuously etched to expose the conductive structure 602. The cap layer 604 can also be etched by changing the etchant having sufficient etching selectivity. Since the cap layer 604 has greater etching rate than the dielectric layers

612 and 606, the cap layer 604 is etched with self-aligned property when the etching process reaches the cap layer 604. The self-aligned manner is also one of features of the invention.

The anti-etch layer 610 mask the void 608 to prevent the void 608 from being open. Here, if one looks into the anti-etch layer 610 in more detail, the anti-etch layer 610 may also be etched a little portion. In the invention, if the indent region is formed by using property of step coverage, the rim region is thinner and could be etched also. Even so, the anti-etch layer 610 also provide a buffer effect, so that the opening 614 do not opening the void 608. This phenomenon may occur in the embodiments of the invention. However, it still has sufficient distance between the anti-etch layer 610 and the void 608 at the rim region. In fact, the area of the anti-etch layer 610 to mask the void 608 and its geometrical structure are the fabrication choices.

Fifth embodiment

In the previous embodiment, the anti-etch layer is included to fill the indent region. However, the anti-etch layer is not absolutely necessary. In Fig. 7A, similar to Fig. 6C, the void 708 is formed in the gap region of the conductive structure 702. The gap region optionally does not extend into the substrate 700. A cap layer 704 is formed on the conductive structure 702. A dielectric layer 706 is formed over the substrate 700 to cover the conductive structure 702 with the cap layer 704. The cap layer 704 including a material, such as doped dielectric, has greater etching rate than the dielectric layer 706. A dielectric layer 710 is formed on the dielectric layer 706. The dielectric layer 710 may also be planarized by, for example, a chemical mechanical

polishing process. In this embodiment, the indent region of the dielectric layer 706 is not filled by a mask layer.

In Fig. 7B, the dielectric layers 710 and 706 are patterned to form an opening 714. When the opening 714 reaches to the cap layer 704, since the cap layer 704 has faster etching rate, the cap layer 704 can be etched with self-aligned property even though the anti-etch layer is absent. Alternatively, the opening 714 can stop on the cap layer 704 first by choosing a first etching selectivity, and penetrate the cap layer by choosing a second etching selectivity. In this alternative manner, the cap layer and the dielectric layer 706 have different etching rates in the two stages. However, the cap layer has the greater etching rate at the second stage.

Figs. 8A-8B are cross-sectional views, schematically illustrating a method to form an interconnect with increased void size, according to the fifth preferred embodiment of the invention. The interconnect structure formed in Fig. 8B is similar to the structure in Fig. 7B. The difference is that the gap region has extended into the substrate 800. In Fig. 8A, the conductive structure 802 is formed on the substrate 800. A cap layer 804 is formed on the conductive structure 802. The dielectric layer 806 is formed over the substrate 800 to cover the conductive structure 804, in which the void 808 exists due to the loose step coverage. A dielectric layer 810 is formed on the dielectric layer 806. The gap region in the conductive structure 802 exposes the substrate 800 and extends into the substrate 800.

In Fig. 8B, the dielectric layers 806 and 810 are patterned to form an opening 814. The opening 814 continuously penetrates the cap layer 804 to expose the conductive structure 802. The cap layer 804 has faster etching rate than the dielectric layer 806. The etching mechanism in Fig. 8B is similar to that in Fig. 7B. If

misalignment occurs, the opening 814 does not open the void 808 due to a faster etching rate on the cap layer 804.

In conclusion, the present invention has several features as follows:

1. The invention uses properties of step coverage by operating at a condition of
5 the loose step coverage or the poor step coverage, so as to form the void at the gap between metal wires with intention. The parasitic capacitance of the interconnect can be effectively reduced.

2. In order to increase the void size, the gap can extend into the substrate.

3. The anti-etching layer 207a is formed above the void to mask the void. As
10 a result, the void is not open.

4. The cap layer 704 is further formed on the conductive structure. The cap layer provides an addition height of the gap region, so as to indirectly increase the void size. The cap layer also allows a self-aligned manner to be performed during fabrication.

15 It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.